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A top-down fabrication process for a-IGZO thin film transistor and patterned organic light-emitting diode

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Abstract−A top-down fabrication process that can simultaneously implement an amorphous indium-gallium-zinc oxide (a-IGZO) thin film transistor (TFT) and an organic light-emitting diode (OLED) device has been studied. The proposed process utilizing self-aligned imprint lithography (SAIL) is simple because it does not require any repetitive alignment and coating steps in the photolithography process for the TFT fabrication. This study reports that a single a-IGZO TFT and OLED device can be fabricated in a top-down manner using the SAIL process. These two devices were fabricated using only imprint lithography and plasma etching processes without any photolithography process, and they were confirmed to operate normally. Although these two devices were studied separately in this report, simultaneous top-down fabrication of an active-matrix OLED pixel composed of a-IGZO TFT and OLED connected together is also possible in principle. The proposed SAIL process is a very easy way to fabricate active-matrix OLED displays, and it can be utilized as an efficient display fabrication process if the few issues mentioned in this study are solved.

Keywords: Self-aligned Process, Imprint Lithography, IGZO, Thin Film Transistor, Organic Light-emitting Diode

INTRODUCTION

Active-matrix organic light-emitting diode (AMOLED) displays consist of a large number of thin film transistors (TFTs) and OLED pixels. To fabricate AMOLED displays, a large number of photolithography processes must be repeatedly performed for defining the TFT patterns and OLED pixel patterns. As the resolution of these displays increases, the alignment problem in successive photolithography processes becomes more and more difficult. Moreover, in the case of a flexible OLED display using a polymer substrate, the alignment of the photolithography process may cause more serious problems due to the inherent properties of the material, such as the high coefficient of thermal expansion of flexible substrates. The fundamental solution to this alignment issue is to avoid the overlay accuracy problem in photolithography by utilizing self-aligned processes. For this purpose, a top-down process called self-aligned imprint lithography (SAIL) has been proposed [1-7]. The SAIL process was originally developed as a method for fabricating TFTs in a self-aligned manner without the use of photolithography. The conventional TFT fabrication process utilizes a bottom-up method in which each layer patterned by photolithography is sequentially stacked upward from the substrate. However, the SAIL process is a top-down method for fabricating TFTs by sequentially etching blanket-deposited multilayer thin films using a three-dimensionally imprinted resin as multiple pre-aligned etch masks. Several studies using this SAIL process for TFT fabrication have been reported [8-13]. The purpose of the SAIL process studied so far is to fabricate a TFT backplain for flat panel displays. However, in order to produce an AMOLED display, an insulator pattern has to be formed on the TFT backplane using an additional photolithography process, and then OLED pixels are separately deposited thereon. The simplest and most convenient method to fabricate an AMOLED display is to eliminate the need for the photolithography process by forming not only TFTs but also OLED pixels using the SAIL process.

The purpose of this study was to develop an efficient process for simultaneously fabricating the TFT and OLED device in a top-down manner using SAIL process. For the TFT and OLED device, a metal-oxide transistor using amorphous indium-gallium-zinc-oxide (a-IGZO) as an active semiconductor and a green-emitting device were used in this study, respectively. In recent years, TFTs for driving flat panel displays tend to mainly utilize the a-IGZO oxide semiconductor due to the high carrier mobility and process convenience. The schematic diagram of the SAIL process carried out in this study is shown in Fig. 1. First, each layer constituting the a-IGZO TFT is sequentially blanket-deposited on a glass substrate, followed by vacuum deposition of a top-emitting OLED device. A resin is spin-coated thereon for imprinting [Fig. 1(a)]. A structure is imprinted on the resin using an imprint stamp prepared in advance as a three-dimensional TFT structure [Fig. 1(b)]. Then, plasma etching is performed to remove the resin pattern with the lowest thickness so that the underlying surface is exposed [Fig. 1(c)]. A structure as shown in Fig. 1(d) can be formed by continuous plasma etching of the exposed surface area down to the glass substrate using various etching gases. In this process, a specific part of the gate thin film can be undercut-etched simultaneously through very fine holes formed in the resin. After removing the thinnest area of the imprinted resin in Fig. 1(d) by etching, the bottom-gate TFT can be formed by etching the OLED and source/drain (S/D) layer through the exposed surface [Fig. 1(e)]. Next, by removing the thinnest part of the remaining resin pattern and the OLED layer underneath [Figs. 1(f) and

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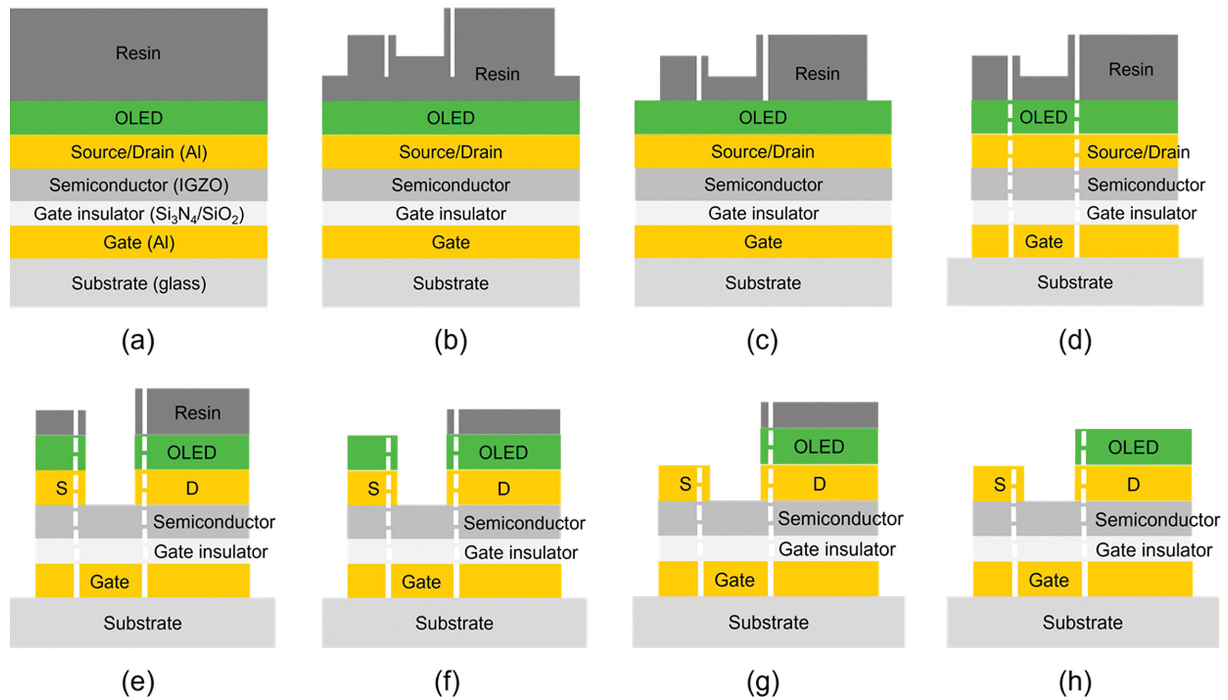

Fig. 1. Schematic diagram of the top-down SAIL fabrication process for the simultaneous fabrication of TFT and OLED: (a) blanket multi-layer coating, (b) resin imprint, (c) resin etch, (d) etching of underlying layers with gate undercut-etch, (e) source/drain separation, (f) resin etch, (g) OLED etch, and (h) resin removal. In (d)-(h), white lines penetrating from top to bottom indicate holes formed in the process of undercut-etching the gate layer. More details on this were explained in Results and Discussion.

1(g)], the final structure [Fig. 1(h)] in which an OLED pixel and TFT are self-aligned can be formed in a top-down fabrication method.

As shown in Fig. 1, the top-down SAIL process of a-IGZO TFT including OLED does not require a photolithography process. Currently, flexible AMOLED displays are manufactured by first coating a heat-resistant polymer film on a glass substrate, forming TFTs and OLED pixels thereon, and finally separating the polymer film from the glass substrate. This is because precise alignment is difficult in a photolithography process when a polymer films is used as a substrate. Therefore, if a self-aligned process, such as the SAIL process is used, this problem can be avoided and ultimately it can be applied to the roll-to-roll manufacturing process of a flexible AMOLED display. This study tried to identify issues that may arise in realizing this process and to examine the feasibility of the process. To this end, a TFT and OLED of the same pattern were fabricated using separate SAIL processes, and the characteristics of each device were evaluated. Finally, problems that occur when both TFT and OLED are fabricated simultaneously by the SAIL process were discussed.

EXPERIMENTAL

After thoroughly cleaning 1 inch×1 inch-sized glass substrates, an aluminum (Al) gate, gate insulating layers, an IGZO semiconductor, a chrome (Cr) protective layer, and an Al S/D electrode were sequentially deposited. These layers are for a-IGZO TFT. For the SAIL process, including an OLED pixel, the Al S/D electrode for the TFT was used as an anode of the OLED pixel, and a green-emitting OLED was deposited on top of the TFT. Then, a silicon nitride (SiN_x) encapsulation layer to protect the OLED was deposited, and a resin to be imprinted with a pattern was finally coated. Table 1 shows the material, deposition method, thickness, and plasma-etching conditions for each layer. As an active semiconductor layer for the TFT, 50 nm-thick a-IGZO layer was deposited using magnetron sputtering. For the deposition, an IGZO target having the composition of $In_2O_3:Ga_2O:ZnO=1:1:1$ mol% was utilized. The resin for imprinting the pattern was NOA63 (Norland, USA). The stamp material for imprinting the pattern was 511RM (Minuta Technology, Korea), which was produced by dropping a few drops on the master template made on a silicon wafer, pressing it with PET film, curing it with ultraviolet (UV) light and then peeling it off. The surface of the stamp was treated with a self-assembled monolayer (octadecyltrichlorosilane) to facilitate peeling after stamping the pattern on the resin on the sample surface. The imprint stamp was placed on the multilayered sample and imprinted using a roll imprint machine. Immediately after imprinting, it was cured for 30 s under UV (1.6-2.0 J/cm^2). After the completion of the first UV exposure, the stamp was removed from the sample and the second exposure was performed on the sample for 60 s to keep the pattern shape and complete curing. Thereafter, the plasma etching processes were sequentially performed under the conditions shown in Table 1.

At each process step, the progress of etching was carefully monitored using an optical microscope, and the completion of each etching step was evaluated by observing the color change of the structure. The structures obtained after each process step were also analyzed by scanning electron microscope (SEM). Electrical char-

Table 1. Materials, deposition methods, thickness, and process conditions for each layer of the sample

	Material	Function	Deposition	Thickness (nm)	Etching condition			Etch rate (nm/min)
					Etching gas	Flow rate (sccm)	RF power (W)	
Resin	NOA63	Imprint resin	spin coating	4,800	Ar	30	50	480
Encapsulation	SiN_x	OLED encapsu-lation	PECVD	200	CF_4	30	70	200
OLED	Al	Cathode	Vacuum evaporation	8	BCl_3/Cl_2	20/5	50	130
	Liq	Electron injection	Vacuum evaporation	1.5				
	Alq_3	Light emission/ Electron transport	Vacuum evaporation	50				
	NPB	Hole transport	Vacuum evaporation	40				
	HATCN	Hole injection	Vacuum evaporation	30				
TFT	Al	S/D electrode	Magnetron sputtering	100	BCl_3/Cl_2	20/5	50	100
	Cr	IGZO protection	Magnetron sputtering	15	Wet etchant	-	-	-
	IGZO	Semiconductor	Magnetron sputtering	50	BCl_3	25	150	16
	SiN_x	Gate dielectric	PECVD	100	CF_4	30	70	27
	SiO_x	Gate dielectric	PECVD	150	CF_4	20	80	36
	Al	Gate electrode	Magnetron sputtering	150	BCl_3/Cl_2	20/5	50	33

acteristics of the fabricated IGZO TFT and OLED were measured using a semiconductor parameter analyzer (Agilent 4155B, USA).

RESULTS AND DISCUSSION

1. Fabrication and Evaluation of a-IGZO TFT by SAIL Process

The three-dimensional TFT structure of the master template fabricated on a silicon wafer is shown in Fig. 2. The master template has a five-layer structure and each layer is 1.5 μm high. The TFT channel is 100×100 μm^2, and small holes are drilled from the surface to the bottom layer. These holes are to reduce the parasitic resistance of the gate electrode and separate the gate line and the S/D line through undercut etching. After UV curing resin was applied and cured on the master template, it was removed to prepare an imprint stamp having the reverse structure of the master template. Separately, the layers constituting the a-IGZO TFT, that is, Al gate, gate insulator, IGZO, Cr, and Al S/D electrode, were sequentially deposited on a glass substrate to prepare a sample. Here, Cr was used to reduce plasma damage to the IGZO thin film during the plasma etching process. Finally, a resin for imprinting the TFT pattern was coated on the S/D electrode surface.

The SAIL fabrication sequence of a-IGZO TFT is shown in Fig. 3. Fig. 3(a) shows the result after imprinting the resin on the sample surface using the imprint stamp. The resulting structure is identical to the master template because it is imprinted with the imprint stamp, which is the opposite structure to the master template. The resin region outside the TFT with the thinnest thickness was first removed by plasma etching to expose the S/D electrode [Fig. 3(b)].

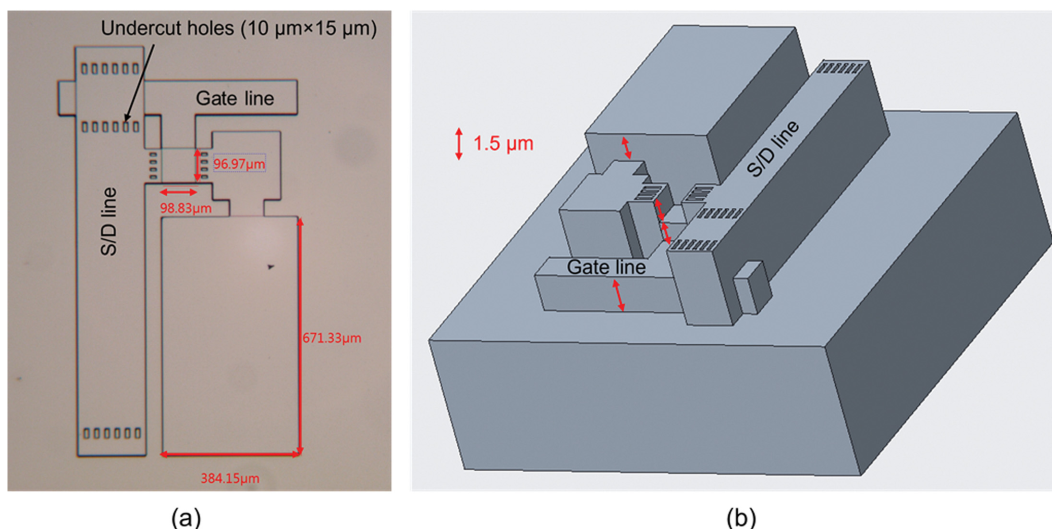

Fig. 2. Dimensions and shape of the three-dimensional master template: (a) top view and (b) side view.

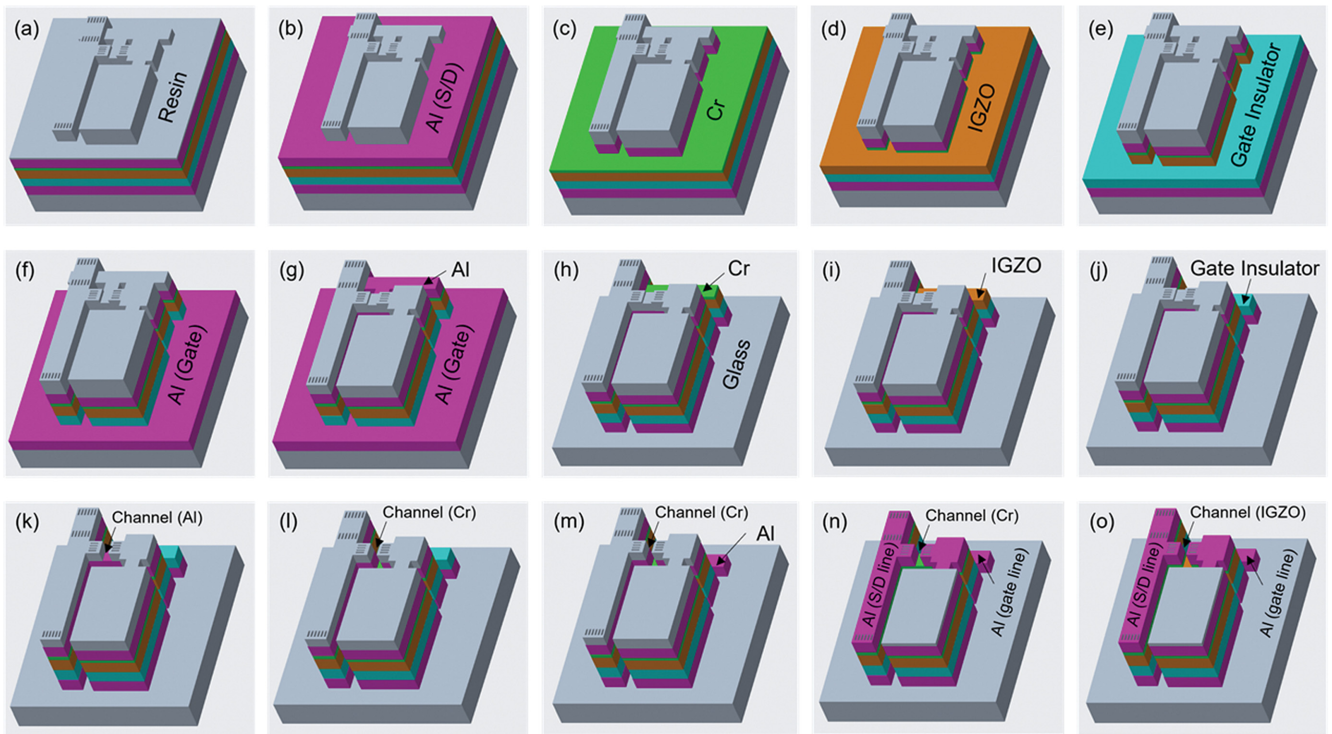

Fig. 3. SAIL process sequence for the fabrication of a-IGZO TFT: (a) imprinting resin, (b) first resin etch, (c) Al etch, (d) Cr etch, (e) IGZO etch, (f) gate insulator etch, (g) second resin etch, (h) Al etch, (i) gate line Cr etch, (j) gate line IGZO etch, (k) third resin etch, (l) channel Al etch, (m) gate line Cr etch, (n) fourth resin etch, (o) channel Cr etch.

Thereafter, the Al S/D electrode, Cr, IGZO, and the gate insulator layers were sequentially removed using plasma etching [Figs. 3(c)-3(f)]. All layers except Cr were removed by plasma etching, but Cr was removed by wet etching. Each plasma etching condition was described in detail in Table 1. Next, as shown in Fig. 3(g), the thinnest resin on the gate line was removed. After removing all the exposed Al thin films at the same time [Fig. 3(h)], the Cr and IGZO layers of the gate line were sequentially etched away [Figs. 3(i) and 3(j)]. After opening the thinnest TFT channel region in the remaining resin structure [Fig. 3(k)], the exposed Al layer in the channel region was removed [Fig. 3(l)]. Next, the gate insulator of the gate line was etched away by plasma etching [Fig. 3(m)], and the remaining resin in the S/D line region was removed [Fig. 3(n)]. Finally, as shown in Fig. 3(o), a-IGZO TFT could be completed by removing Cr in the channel region. Cr was used as a protective layer on top of IGZO because Cr has a relatively low plasma-etching rate compared to other materials, so it is advantageous to protect the surface of IGZO layer in several different plasma etching processes. The IGZO surface, which is most important for the TFT operation, can be stably protected by Cr during the SAIL process, but eventually the Cr layer in the channel region must be removed. If the Cr layer is plasma-etched in the final process, the IGZO surface may be damaged by plasma. For this reason, in this study, the Cr layer was inevitably removed by wet etching with a Cr etchant. As described here, it is possible to fabricate an a-IGZO TFT in a top-down manner by using a three-dimensional resin structure as multiple pre-aligned etch masks without a photolithography process. This SAIL process has the advantage that a roll-to-roll process using a flexible polymer substrate is possible because all structures are self-aligned and the process consists only of an imprint process and plasma etching processes compatible with the roll-to-roll process.

The SAIL process shown in Fig. 3 was carried out sequentially and the optical microscope images of the corresponding structure obtained after each step are shown in Fig. 4. The photographic top-view images in Figs. 4(a)-4(o) match the structures in Figs. 3(a)-3(o), respectively. Although each three-dimensional structure cannot be confirmed with the top-view images shown in Fig. 4, the changes after each process can be distiguished by the difference in color. Fig. 4(o), the final TFT structure, shows that the gate line, S/D line, and IGZO channel are all formed as designed. As described above, since the small holes formed inside the TFT are drilled down to the lowest level of the resin, the color inside the holes after each process is always the same as that outside the TFT pattern. The purpose of arranging these holes is not only to reduce the capacitance of the electric interconnection by shorting the S/D and gate lines, as well as to reduce the parasitic capacitance of the TFT by disconnecting the left and right sides of the gate electrode. When the bottom Al gate electrode is finally etched, the Al lines can be disconnected by undercut etching with the etch gases supplied through the holes. Fig. 4(p) shows the bottom Al structure observed from the transparent glass substrate, and it can be seen that the Al line is disconnected by the undercut etching. In Figs. 1(d)-1(h), the white lines penetrating from the top to the bottom of the TFT structure represent these undercut holes. This SAIL process is very advantageous in terms of process convenience. If a TFT as shown in Fig. 4 is fabricated in a conventional bottom-up process, a large num-

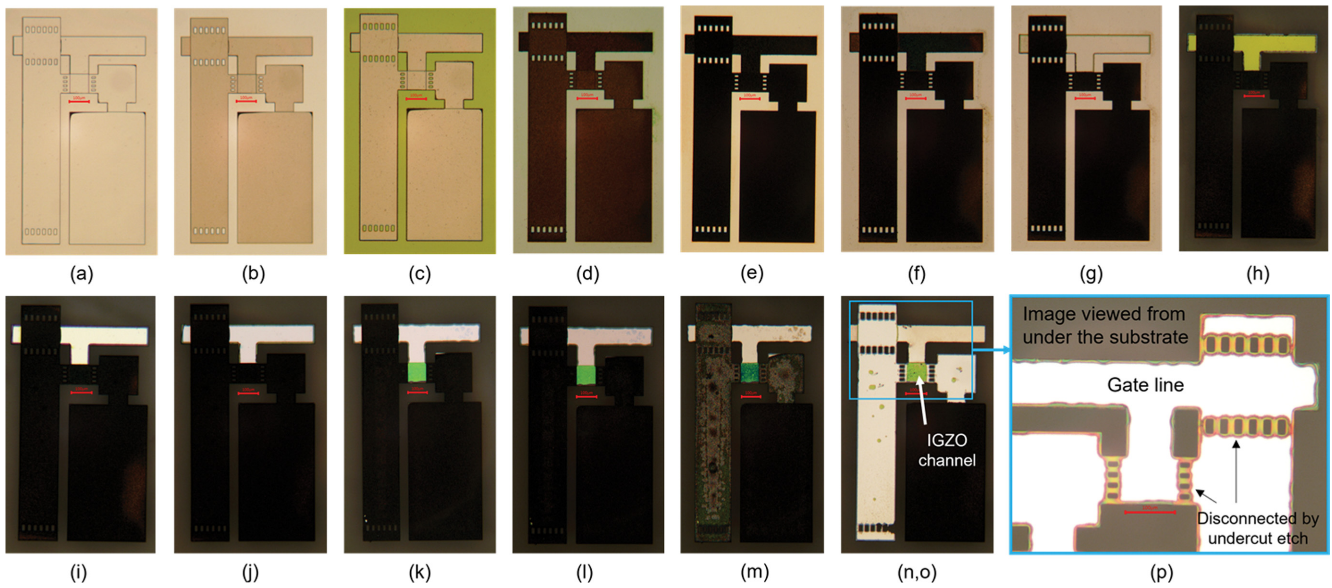

Fig. 4. Actual photographic images after each process shown in Fig. 3: (a) imprinting resin, (b) first resin etch, (c) Al etch, (d) Cr etch, (e) IGZO etch, (f) gate insulator etch, (g) second resin etch, (h) Al etch, (i) gate line Cr etch, (j) gate line IGZO etch, (k) third resin etch, (l) channel Al etch, (m) gate line Cr etch, (n,o) fourth resin etch and channel Cr etch, and (p) image viewed from under the glass substrate.

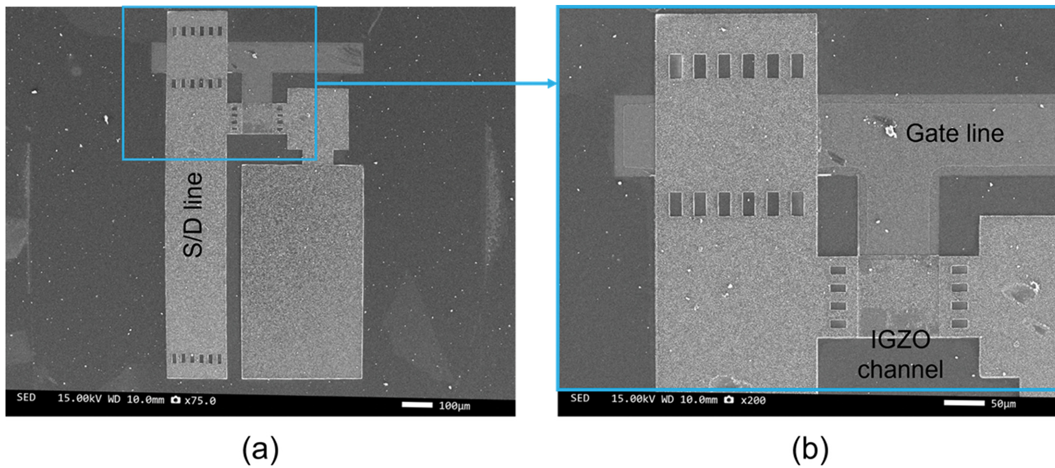

Fig. 5. (a) SEM image of the fabricated a-IGZO TFT and (b) an enlarged image around a-IGZO channel.

ber of step-by-step photolithography and deposition processes are required. However, since the SAIL process requires only one imprint process and a continuous plasma etching process, it is possible to fabricate the TFT much more easily.

Fig. 5 shows SEM images of a-IGZO bottom-gate TFT that has been fabricated. As can be seen in the enlarged image, the gate electrode underneath the IGZO channel separated by small holes on the left and right sides of the channel. The gate line is located at the lowest level and is separated from the S/D line at the highest level. In addition, in order to reduce the signal delay that may occur in the electrode interconnection, the gate line is also separated by small holes above and below the gate line. As shown in the figure, the maximum thickness of TFT is 565 nm including both gate electrode and S/D electrode, and the height difference between each layer of the TFT is as thin as several hundred nanometers.

Fig. 6(a) shows a typical transfer characteristics of TFT with the channel width of 100 μm and length of 100 μm, fabricated by the SAIL process. The fabricated TFT showed clean switching behavior as shown in the figure. The drain voltage was set to 5 V, and the gate voltage was swept from −15 V to 30 V. The device demonstrates the enhancement mode characteristic with the threshold voltage of 1.5 V. Fig. 6(b) shows the TFT output characteristic curves measured with varying drain voltage from 0 V to 20 V and gate voltage from 0 V to 30 V with a step of 5 V. The electrical property of the a-IGZO TFT fabricated by the SAIL process was a linear mobility of 1.1 $cm^2/V\cdot s$, and a current on/off ratio of 1.2×10^6.

2. Fabrication and Evaluation of Patterned OLED by SAIL Process

The patterned OLED device was fabricated in a top-down method using the SAIL process, and its characteristics were evaluated. First,

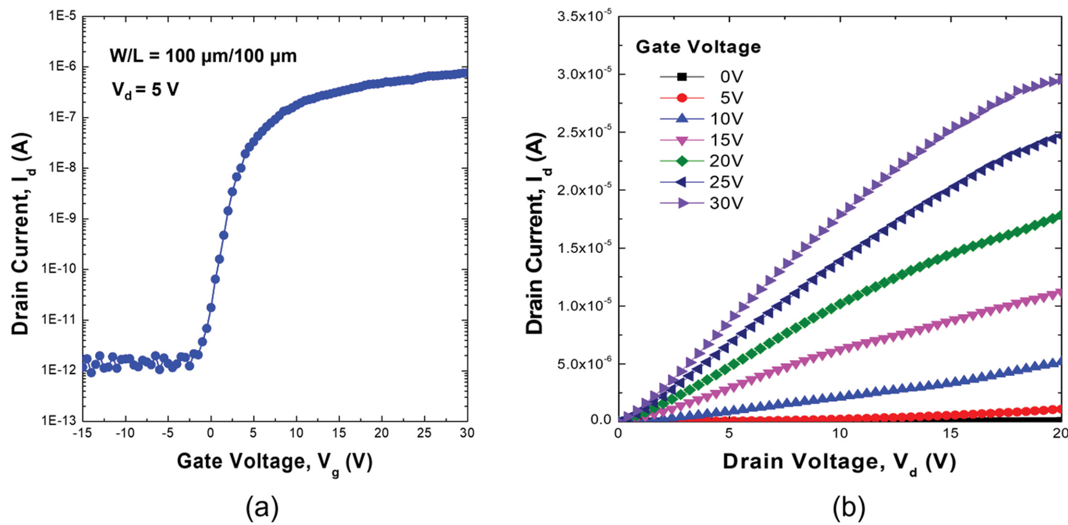

Fig. 6. Characteristic curves of a-IGZO TFT fabricated in this study: (a) transfer curve, (b) output curve.

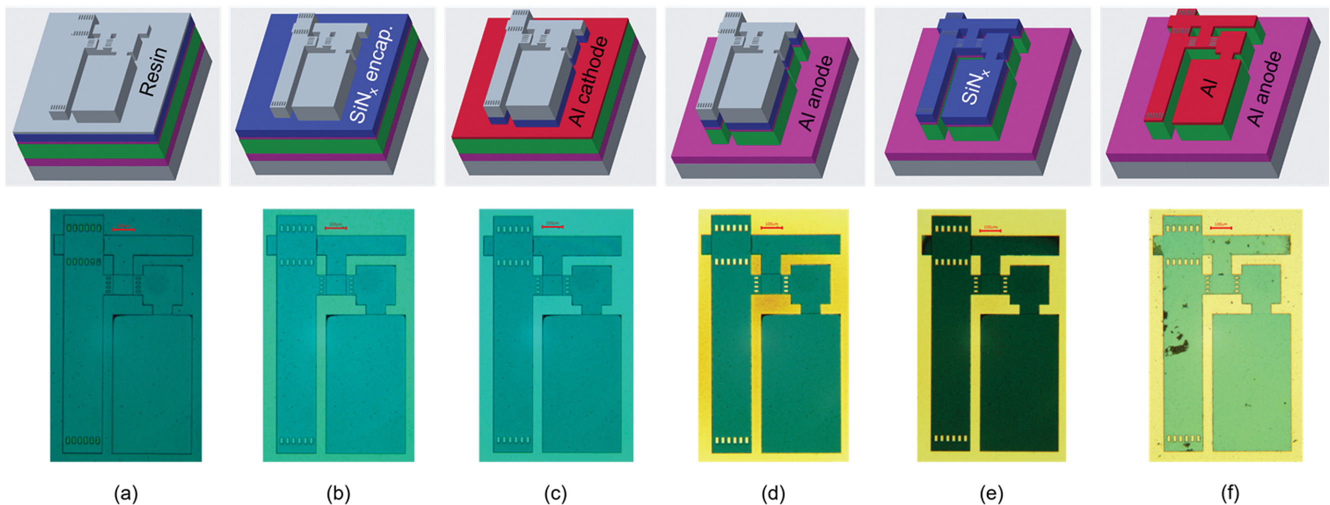

Fig. 7. SAIL process sequence and corresponding photographic images after each process: (a) imprinting resin, (b) first resin etch, (c) SiN$_x$ etch, (d) Al cathode etch, (e) resin removal, (f) SiN$_x$ etch.

an Al anode was coated on a glass substrate. An OLED device and an Al cathode were vacuum-deposited thereon, and then a SiN$_x$ encapsulation layer was deposited by plasma-enhanced chemical vapor deposition (PECVD). After a resin was finally applied, a TFT pattern was formed by imprinting with the same stamp as before. Fig. 7 shows the process configuration and corresponding photographic images of each stage in the SAIL process to fabricate a TFT-patterned OLED device. The photographic images appear green because the green-emitting OLED is deposited on the samples. Fig. 7(a) shows the image after the imprint process is finished. After removing the thinnest resin area outside the TFT pattern by plasma etching [Fig. 7(b)], the exposed SiN$_x$, Al cathode, and OLED layers were etched away in order [Figs. 7(c) and 7(d)]. Unlike the TFT SAIL fabrication process, the five-layer resin pattern was removed at once in the fifth stage [Fig. 7(e)] to form a patterned OLED as shown in Fig. 7(f). Although not described in detail in this figure, the Al electrode has a large work function, so it is not suitable as an anode of an OLED device. A 1,4,5,8,9,11-hexaazatriphenylene-hexacarbonitrile (HATCN) material was used as the hole injection layer to facilitate the injection of holes from the Al anode. All the organic layers, HATCN, N,N′-di(1-naphthyl)-N,N′-diphenyl-(1,1′-biphenyl)-4,4′-diamine (NPB), tris(8-hydroxyquinolinato)aluminum (Alq_3), and 8-hydroxyquinolinolato-lithium (Liq), constituting the OLED could be easily etched with a BCl_3 and Cl_2 mixed etching gas. The purpose of this process is to confirm that it is possible to fabricate without damaging the side of the OLED pattern during the plasma etching processes. As can be seen in Fig. 7(f), it was confirmed that the OLED, shown in green color, was fabricated without damage to the pattern edges. This is possible because during the plasma etching process of the SAIL process, the OLED is protected by the resin thereon, and each layer of the OLED is anisotropically removed by the reactive ion etching. As shown in Fig. 8, the fabricated OLED showed the green emission according to the designed pattern even though it was exposed to several plasma

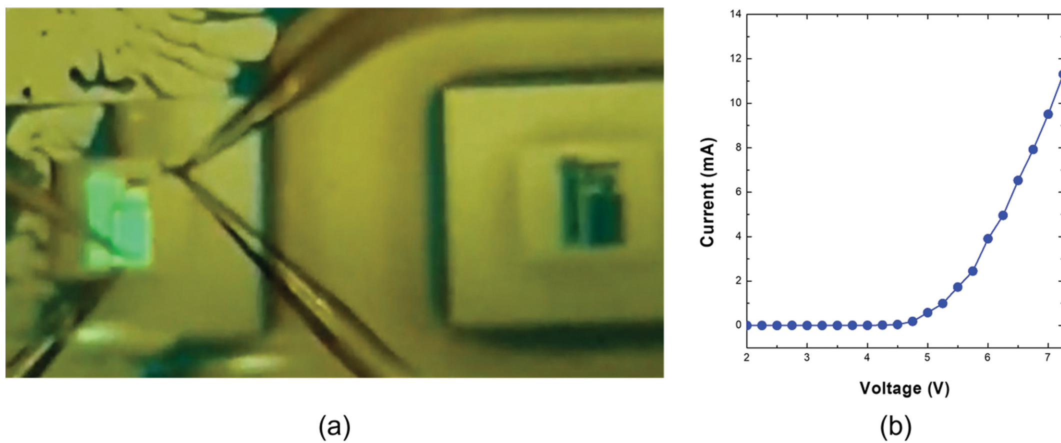

Fig. 8. (a) Photographic image of a patterned OLED device in operation, (b) current-voltage curve of the patterned OLED showing the diode characteristic.

etching processes. Since the light-emitting area was very small, the OLED had to be driven in the probe station, which made it impossible to measure the luminance directly. However, it was possible to confirm with an optical microscope that the emission occurred according to the fabricated pattern [Fig. 8(a)]. The current measured at the applied voltage shows typical diode characteristics as shown in Fig. 8(b).

3. Simultaneous Top-down Fabrication of a-IGZO TFT and OLED Pixel by SAIL Process

As described above, both a-IGZO TFT and OLED device were able to be fabricated using the top-down SAIL process. If all the layers constituting the TFT and OLED can be properly etched, simultaneous top-down fabrication of TFT-connected OLED pixels should be possible considering the principle of the SAIL process. For simultaneous fabrication, a-IZGO TFT layers and OLED were sequentially deposited on the top of the glass substrate as shown in Fig. 9(a), and then the resin was finally coated. Although omitted in this figure, a thin Cr layer exists between the S/D Al and IGZO layers. The role of this Cr layer is to prevent plasma damage of IGZO surface when the TFT channel is opened by plasma-etching Al. As previously described in section (a), Cr was able to be removed without damage to IGZO using a wet etchant (ETCR-400, solution of cerium ammonium nitrate and perchloric acid). Fig. 9(b), a sample image after imprinting, shows green color because green-emitting OLED is deposited over the entire area. Figs. 9(b)-9(e) show the images after the resin, SiN_x encapsulation layer, and Al cathode/OLED/Al anode are sequentially etched outside the TFT pattern. However, in the process of wet etching the exposed Cr layer, the OLED was damaged from the pattern boundary by the etchant solution. This result can be confirmed by color change as shown in Fig. 9(f). This figure shows that the OLED area, which appears in green, has been eroded by the etchant solution from the boundary. To prevent such OLED erosion, wet etching should be replaced with plasma dry etching. However, since plasma etching of the Cr layer also causes damage to the a-IGZO semiconductor, a new method to solve this problem must be devised. An alternative is to use a conductive polymer instead of the Cr layer. A prerequisite for this material is that it should be able to be removed by a wet process without affecting the OLED.

In summary, each of the a-IGZO TFT and OLED devices can be fabricated using the SAIL process, but the simultaneous fabrication was not successful due to the damage issue of the IGZO layer. Although the process of fabricating an OLED pixel including a-IGZO TFT by the top-down SAIL process was not successful at the current

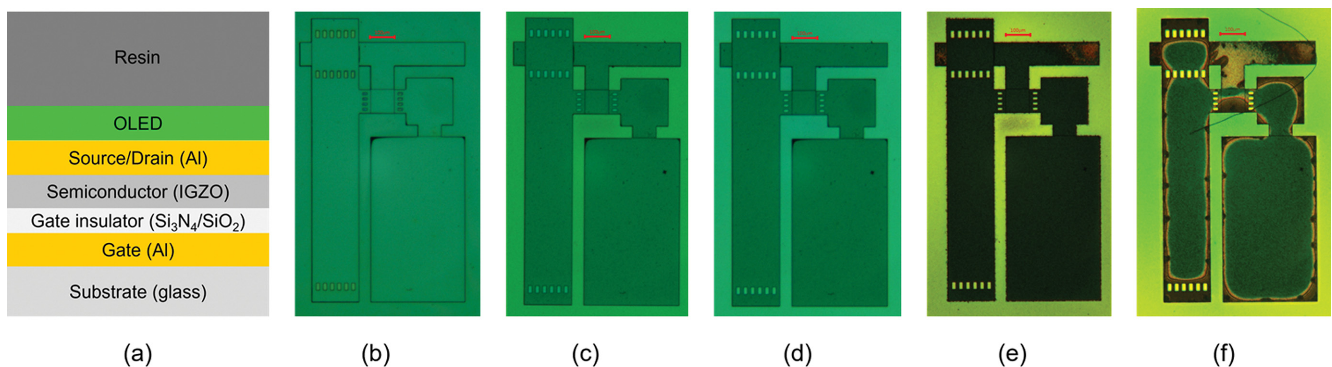

Fig. 9. SAIL process sequence and corresponding photographic images after each process: (a) cross-sectional structure, (b) imprinting resin, (c) first resin etch, (d) SiN_x encapsulation layer etch, (e) Al cathode/OLED/Al anode etch, (f) Cr wet etching.

research stage, when a solution to the damage issue of the IGZO layer is found, the process proposed in this study will become a future production technology that can easily and simply manufacture AMOLED displays in a self-aligning method. Ultimately, this process could be utilized in the mass production of large-area AMOLED displays using a roll-to-roll process on a flexible polymer substrate.

CONCLUSIONS

With the SAIL process, a-IGZO TFT and OLED were fabricated by an imprint process and a continuous plasma etching process in a top-down manner. This process has the advantage of being able to easily fabricate a TFT by using a three-dimensional imprint pattern as muliple pre-aligned etch masks without using a photolithography process in the TFT manufacturing process, where overlay accuracy is very important. It was confirmed that a-IGZO TFT fabricated by the SAIL process showed normal switching behavior. An OLED device with the same pattern was also fabricated using the top-down SAIL process and showed that it operates normally according to the imprinted pattern shape. However, the SAIL process, which simultaneously fabricates a combined structure of a-IGZO TFT and OLED, was not successful in this study. The reason is due to the absence of an etching method that can simultaneously protect the OLED material and the a-IGZO material of the TFT. Except for this one problem, the feasibility of the SAIL process has been fully confirmed in this study, so the resolution of this problem may open a new way for top-down production of AMOLED displays. In particular, this SAIL process is expected to be important for manufacturing flexible AMOLED displays using a roll-to-roll process, because only the imprint process and plasma etching process suitable for the roll-to-roll process are used without a photolithography process.

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CRediT AUTHORSHIP CONTRIBUTION STATEMENT

Hyungki Park: Data curation, Formal analysis, Investigation. **Changyun Na:** Investigation, Methodology. **Hangil Lee:** Invertigation, Visualization. **Sung Min Cho:** Conceptualization, Funding acquisition, Supervision, Writing - original draft.

DECLARATION OF COMPETING INTEREST

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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