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Simplified design of proportional-integral-derivative (PID) controller to give a time domain specification for high order processes

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Abstract−An efficient simplified method is proposed for the time domain design of industrial proportional-integral-derivative (PID) controllers and lead-lag compensators for high order single input single output (SISO) systems. The proposed analytical method requires no trial error steps for a lead-lag compensator design in the time domain by using the root-locus method. A practical PID controller design method was obtained based on the corresponding lead-lag compensator to give a required time-domain specification. Simulation studies were carried out to illustrate the control performance of the controllers by the proposed method. The proposed PID controller and lead-lag compensator directly satisfied time domain control specifications such as damping ratio, maximum overshoot, settling time and steady sate error without trial and error steps. The suggested algorithm can easily be integrated with a toolbox in commercial software such as Matlab.

Keywords: PID Controller, Lead-lag Compensator, Time-domain Control Specification, Dead-time System, Root Locus

INTRODUCTION

Proportional-integral-derivative (PID) controllers are used in more than 90% of today's industrial applications as the dominant form of feedback controllers [1-3]. PID controllers have also been most commonly used for process control applications. The design of PID controllers may be based on either the frequency domain, using tools such as Bode-plot, or the time domain, using tools such as roots-locus. In the frequency domain-based design, the control performance specifications are usually given in terms of gain margin, phase margin, gain crossover frequency, peak resonance and so on, whereas performance in the time domain is specified in terms of peak time, maximum percentage overshoot, rise time, peak time, settling time and steady state error. Lead-lag compensators can also be used as an alternative to PID controllers to mitigate the delicacies of PID controllers such as noise interference and windup effects [4,5].

Since lead-lag compensators are a general case of PID controller, the same procedure used for the lead-lag design can also be used to design PID controllers. To date, most of the control designs for lead-lag compensators have been in the frequency domain: Wang proposed an approach for phase-lead-lag compensators which achieves desired specifications of gain and phase margins for all-pole stable plants with time-delay [6]. Zanasi et al. proposed a lead-lag compensator design approach based on an analytical and graphical procedure design on the Nyquist and Nichols planes, which satisfies frequency domain specifications of phase margin, gain margin and phase or gain crossover frequency [7]. Yeung et al. suggested a universal design chart for lag-lead compensators, which allows for the design of compensators without trial and error, while meeting four specifications: steady-state error, phase margin, gain margin, and gain (or phase) crossover frequency [8]. For further works about lead-lag compensators in frequency domain, readers can refer to [9-15].

Control design using time domain performance and procedures has a number of advantages because it is directly related to the time domain specifications, such as damping ratio, maximum overshoot, rise, peak and settling time. Moreover, the time domain based design procedure can also be used to solve control actions which meet frequency domain specifications, such as gain and phase margin, and resonant peak. This is possible thanks to the relationship between frequency domain and time domain. The control design in the time domain is mainly based on the root locus technique [16]. Famous control textbooks [16,17] provide a basic procedure for the design of lead-lag compensators in the time-domain. However, to date, papers which deal with the design of PID controllers as well as lead-lag compensators using the root-locus method are rare e.g. [18-20].

In this paper, we propose a simple and systematic design method of PID controllers in the time domain for high order SISO systems. The proposed design method is based on the design of the corresponding lead-lag compensator. As mentioned, since most lead-lag control designs to date are based on frequency domain design specifications and procedures, a time domain design of the lead-lag compensator is proposed by using the root-locus method. With the proposed design algorithm, one can easily complete the control design operation only by entering the time domain specifications: the damping ratio or maximum overshoot, the desired settling time, and the desired steady state error, etc. After entering the control specifications, the algorithm automatically finds the desired PID controller parameters that meet the specified requirements. Differently from other experimental methods [21,22] and existing

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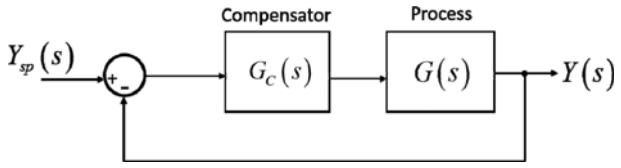

Fig. 1. Feedback control system.

optimization techniques for obtaining the PID controller parameters [21,23-30], the unique and beneficial feature of the proposed PID design is the automatic gain selection algorithm that meets predetermined time domain criteria (rise time, maximum overshoot, damping ratio, settling time, steady state response, etc.). The main contribution of this work, that differs from those in [18-20], is the extension and the generalization of the concept therein for a systematic design of higher order SISO time delay systems in time-domain.

The remainder of this paper is organized as follows: the lead-lag compensator design procedure in time domain is shown in section 2, the PID controller derived from the lead-lag compensator technique is presented in section 3, section 4 is dedicated to simulation results, and a conclusion of the paper is given in section 5.

LEAD-LAG COMPENSATOR DESIGN IN THE TIME DOMAIN FOR HIGH ORDER SISO SYSTEMS

A typical lead-lag compensator system is shown in Fig. 1. Lead-lag compensators, like any kind of controllers, aim to bring the system's output to a desired response. As its name suggests, the goal of a compensator is to compensate a performance deficiency by altering the shape of the frequency response or the root-locus path.

The time domain based design of lead-lag compensators is mainly based on reshaping the root-locus so that the new loci of the closed-loop system pass through the designer's desired poles. A general n-order SISO dead-time system is given in Eq. (1); the system consists of n poles $(p_i)_{i=1,n}$ and m zeros $(z_i)_{i=1,m}$; K and θ represent the gain and the dead-time of the nominal process, respectively.

$$G(s)=\frac{K\Pi_{i=1}^{m}(s+z_i)}{\Pi_{i=1}^{n}(s+p_i)}e^{-\theta s} \tag{1}$$

The lead-lag compensator transfer function consists of a lead part and a lag part, and can be written as follows:

$$G_c(s)=G_{LeadLag}(s)=K_{cLead}\frac{s+z_{cLead}}{s+p_{cLead}}K_{cLag}\frac{s+z_{cLag}}{s+p_{cLag}} \tag{2}$$

To design a lead-lag compensator using a similar procedure to that described in [16], the dead-time has to be approximated using a Taylor series approximation [31] or a Pade approximation [32]. Using the Pade first order approximation, for example, the dead-time of the system can be approximated as

$$e^{-\theta s}\approx\frac{2-\theta s}{2+\theta s} \tag{3}$$

A general SISO dead-time system can then be approximated as follows:

$$G(s)=\frac{K\Pi_{i=1}^{m}(s+z_i)}{\Pi_{i=1}^{n}(s+p_i)}e^{-\theta s}\approx\frac{K\Pi_{i=1}^{m}(s+z_i)}{\Pi_{i=1}^{n}(s+p_i)}\frac{2-\theta s}{2+\theta s} \tag{4}$$

The plant can also be written in the following shortened form

$$G(s)=-G_0(s)\left(\frac{s-z_{DT}}{s+p_{DT}}\right) \tag{5}$$

where G_0 is the nominal plant without dead-time; z_{DT} and p_{DT} are the zero and pole, respectively, brought about by the dead-time term. G_0, z_{DT} and p_{DT} are given as

$$G_0(s)=\frac{K\Pi_{i=1}^{m}(s+z_i)}{\Pi_{i=1}^{n}(s+p_i)};\ z_{DT}=p_{DT}=2\theta^{-1} \tag{6}$$

The open loop transfer function is given as

$$G_{ol}(s)=G_cG=-G_cG_0\left(\frac{s-z_{DT}}{s+p_{DT}}\right) \tag{7}$$

The main design concept behind the lead part of the lead-lag compensator is to force the root-locus to pass through the desired closed-loop pole. The initial stage is to calculate the desired location of the closed-loop pole, based on pre-determined time domain specifications.

1. Calculation of the Desired Closed-loop Pole Location

Let s_d be a desired closed-loop pole location; s_d is obtained from the time domain specifications. For example, let the time domain specifications be given in terms of the damping ratio ζ and the settling time t_s. First, the specifications are translated into the desired closed-loop pole location in the s plane. If the desired control goal is to decrease the settling time, t_s, while maintaining the same damping ratio ζ (keeping same maximum overshoot), the desired location of the closed-loop pole will belong to the line ζ=cste, as shown in Fig. 2.

Let t_{sd} be the desired settling time of the system under control. The desired closed-loop pole location can be decided by the designer without using the technique in this subsection. Once the desired location of the closed-loop pole is fixed, the desired settling time of the system is automatically related to this desired closed-loop pole. For a higher order system, the relationship between this pole

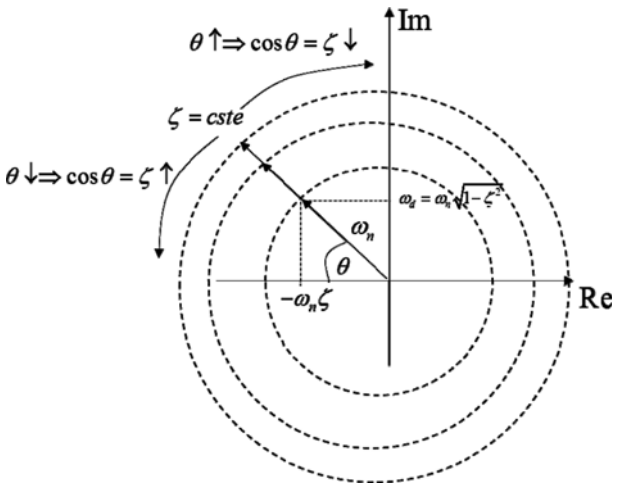

Fig. 2. S-plane pole location.

location and the desired settling time should first be evaluated before using the results in this work. But for the sake of simplification, and without loss of generality, if we assume the higher order system has a dominant pair of poles, it can hence be approximated by a second-order system. In this case, the relationship between the damping ratio, natural frequency of the system, and the desired closed-loop pole can be given as in Eq. (8), for a settling time definition corresponding to 5% of the final value.

$$t_s \approx \frac{4}{\zeta\omega_n};\ t_{sd} \approx \frac{4}{\zeta_c\omega_{nc}} \tag{8}$$

where ζ and ω_n are the damping ratio and the frequency, respectively, of the uncompensated system, whereas ζ_c and ω_{nc} are the damping ratio and the frequency, respectively, of the compensated system. Let $\alpha>1$ be the decrease in ratio of the settling time. The desired settling time of the system can be expressed in terms of the settling time of the uncompensated stable system as $t_{sd}=t_s/\alpha$. The relationship between the settling time of the system without a controller and that of the compensated system can be given as follows:

$$t_{sd} \approx \frac{4}{\zeta_c\omega_{nc}} = \frac{t_s}{\alpha} = \frac{4}{\alpha\zeta\omega_n} \tag{9}$$

In the case of damping ratio, $\zeta_c=\zeta$, the relationship between the compensated frequency and the natural frequency can be given as follows:

$$\omega_{nc}=\alpha\omega_n \tag{10}$$

Note that since $\alpha>1$, the new compensated frequency, ω_{nc}, is higher than the natural frequency, ω_n. Thus, as α increases, the new desired settling time decreases, but the frequency of the system increases, and this may bring the system to instability for higher values of α. This tradeoff should be considered during the design phase of the compensator. After ω_{nc} is calculated, the compensated damped frequency, ω_{dc}, can be calculated as follows:

$$\omega_{dc}=\omega_{nc}\sqrt{1-\zeta_c^2} \tag{11}$$

The desired pole location, s_d, can now be calculated as follows:

$$s_d=-\zeta_c\omega_{nc}\pm j\omega_{dc} \tag{12}$$

The desired closed-loop pole, s_d, above, can also be rewritten in terms of the desired settling time, t_{sd}, as follows:

$$s_d=-\frac{4}{t_{sd}}\pm j\omega_{dc} \tag{13}$$

where j is the complex number, $j^2=-1$.

Once the desired closed-loop location of the system has been calculated, the next step is to reshape the root-locus, forcing it to pass through the desired closed loop poles.

Note that, in this paper, the desired settling time of the compensated system was related to that of the uncompensated system only for the sake of simplification. However, the main important control parameter is the position of the desired close-loop pole. Once the desired close-loop pole is fixed by the control designer, the desired settling time is derived from this. For a higher order system, such derivation of the settling time from the closed-loop pole location can be obtained numerically.

2. Design of the Lead Part of the Lead-lag Compensator

As mentioned, the main goal of the lead compensator is to reshape the root-locus so that it passes through the desired closed-loop pole. The desired closed-loop pole, s_d, belongs to the root-locus if the following relationship is satisfied:

$$1+G_{ol}(s_d)=0 \Rightarrow 1-G_c(s_d)G_0(s_d)\left(\frac{s_d-z_{DT}}{s_d+p_{DT}}\right)=0 \tag{14}$$

Eq. (14) can be rewritten in the expanded form:

$$K_{cLead}\frac{s_d+z_{cLead}}{s_d+p_{cLead}}\times\frac{K\Pi_{i=1}^{m}(s_d+z_i)}{\Pi_{i=1}^{n}(s_d+p_i)}\left[-\frac{s_d-z_{DT}}{s_d+p_{DT}}\right]=-1 \tag{15}$$

The term in the square bracket in Eq. (15) results from the contribution of dead-time. For $K_{cLead}>0$ and $K>0$, the angle relationship of Eq. (15) can be written as:

$$\angle(s_d+z_{cLead})-\angle(s_d+p_{cLead})+\angle G_0(s_d) + [\angle(s-z_{DT})-\angle(s+p_{DT})+\pi]=\pi \tag{16}$$

Referring to Eq. (6), the angle of the nominal system transfer function at the desired pole location, $\angle G_0(s_d)$, is given as:

$$\angle G_0(s_d)=\Sigma_{i=1}^{m}\angle(s_d+z_i)-\Sigma_{i=1}^{n}\angle(s_d+p_i) \tag{17}$$

The angle of the compensator, θ_c, is defined as:

$$\theta_c=\angle(s_d+z_{cLead})-\angle(s_d+p_{cLead})=\theta_{zc}-\theta_{pc} \tag{18}$$

where $\theta_{zc}=\angle(s_d+z_{cLead})$ is the angle from the compensator zero to the desired closed-loop pole, and $\theta_{pc}=\angle(s_d+p_{cLead})$ is the angle from the compensator pole to the desired closed-loop pole, as shown in Fig. 3.

Using Eqs. (16), (17) and (18), the angle of the lead compensator for the approximated high order SISO dead-time system is written as:

$$\theta_c=-\Sigma_{i=1}^{m}\angle(s_d+z_i)+\Sigma_{i=1}^{n}\angle(s_d+p_i)-\angle(s-z_{DT})+\angle(s+p_{DT}) \tag{19}$$

The term in square brackets in Eq. (16) is brought about by the dead-time term. If the dead-time has not been taken into account during the design of the compensator, the angle of the compensator is given as

$$\theta_c=\pi-\angle G_0(s_d)=\pi-\Sigma_{i=1}^{m}\angle(s_d+z_i)+\Sigma_{i=1}^{n}\angle(s_d+p_i) \tag{20}$$

Once the angle of the compensator has been calculated, the next

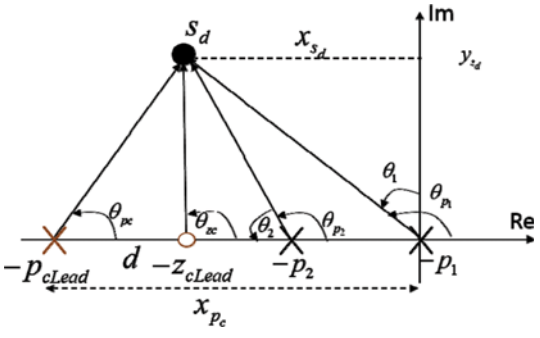

Fig. 3. Location of the pole and zero of the lead compensator.

step is to determine the location of the pole and zero of the lead compensator [16]. The zero of the compensator should be placed on the negative real axis, on the same vertical line as the desired closed-loop poles. To illustrate the calculation of the position of the zero, z_{cLead}, and the pole, p_{cLead}, of the compensator, let us refer to Fig. 3 without loss of generality.

Fig. 3 is a representation of a lead compensator for an SISO system with two poles, where one pole, p_1, is located at the origin. Since z_{cLead} is placed nearly on the vertical line that passes through s_d, then the angle, θ_{zc}, from the zero to the desired closed-loop pole is nearly $\pi/2$ rad. After calculating the compensator's angle, θ_c, the proposed algorithm for the placement of the compensator's zero is as follows:

$$\text{if } \theta_c < \frac{\pi}{2}$$
$$z_{cLead} = |x_{sd}| + \varepsilon = \zeta\omega_n + \varepsilon \quad (21)$$
$$\text{else}$$
$$z_{cLead} = |x_{sd}| - \varepsilon = \zeta\omega_n - \varepsilon$$

where $x_{sd}=\mathrm{Re}(s_d)$ is the real part of the desired closed-loop pole, s_d, and ε is a small number which can be used as a tuning parameter of the lead compensator. Once the zero of the compensator has been located, the pole of the compensator can be calculated using a simple trigonometric relationship. Referring to Fig. 3, the distance, d, between the zero and the pole of the lead compensator can be found as follows:

$$d = \frac{y_{sd}}{\tan\theta_{pc}} \quad (22)$$

where

$$\theta_{pc} \approx 90 - \theta_c \quad (23)$$

And $y_{sd}=\mathrm{Im}(s_d)$ is the imaginary part of the desired closed-loop pole s_d. Finally, the pole of the compensator can be written as

$$p_{cLead} = z_{cLead} + d \quad (24)$$

Once z_{cLead} and p_{cLead} have been calculated, the gain of the lead compensator, K_{cLead}, can be calculated by taking the norm condition of Eq. (15). K_{cLead} can be determined as follows:

$$K_{cLead} = \frac{|s_d + p_{cLead}|\Pi_{i=1}^{n}|s_d + p_i|}{|K||s_d + z_{cLead}|\Pi_{i=1}^{m}|s_d + z_i|} \frac{|s + p_{DT}|}{|s - z_{DT}|} \quad (25)$$

After calculating z_{cLead}, p_{cLead} and K_{cLead}, the lead part of the compensator can then be calculated as follows:

$$G_{Lead} = K_{cLead}\frac{s + z_{cLead}}{s + p_{cLead}} \quad (26)$$

3. Design of the Lag Part of the Lead-lag Compensator

Similar to the notation used for the lead compensator, the lag compensator can be described as

$$G_{Lag} = K_{cLag}\frac{s + z_{cLag}}{s + p_{cLag}} \quad (27)$$

The design of the lag compensator can be divided into two parts: the design of the location of the poles and zeros of the compensator, and the design of the compensator gain.

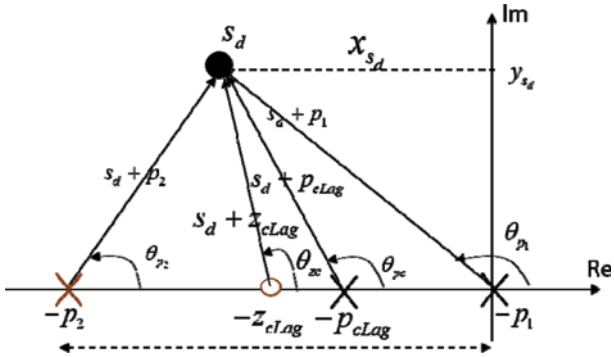

Fig. 4. Location of the pole and zero of the lag compensator.

3-1. Design of the Pole-zero Location of the Lag Compensator

The goal of a lag compensator is to improve steady state performance without affecting transient response. To reduce the steady state error without affecting the transient response of the system, the angle of the lag compensator, θ_{cLag}, must be as small as possible. Similar to Eq. (18), and referring to Fig. 4, the angle of the compensator can be defined as

$$\theta_{cLag} = \theta_{zc} - \theta_{pc} \quad (28)$$

For the angle of the compensator to be as small as possible, the condition $\theta_{zc} \approx \theta_{pc}$ must be satisfied. This condition can only be met if the pole and zero, p_{cLag} and z_{cLag}, of the compensators are close to one another. This condition is critical when designing the lag compensator. After the zero and the poles of the compensator are fixed closed to each other, the remaining variable to determine is K_{cLag}. To be able to do so, the maximum allowable steady state error, e_{ss}, must first be defined. Also, the gain of the lag compensator will depend on the system type. By definition, if the open loop transfer function is given as:

$$G_{ol} = \frac{N(s)}{s^n D(s)} \quad (29)$$

where N(s) and D(s) are polynomials in s, and s^n represents all the powers of s that can be factored from the denominator, then the system is of type n. The type of the system is important, as it determines the type and the trend of the steady state error of the system, depending on the type of system input. For type 1 systems, there may be no need to build a lag compensator for a step input, as the steady state error will always be zero, even without the use of a lag compensator. In this case, to determine the compensator gain, K_{cLag}, the steady state error of the system due to some other input, such as ramp input, can be used to determined K_{cLag}. Using the final value theorem, the steady state error of the feedback control system in Fig. 1 can be defined as follows:

$$e_{ss} = \lim_{t\to\infty} e(t) = \begin{cases} \dfrac{1}{1 + \lim\limits_{s\to 0} GG_c} & \text{for step input} \\ \lim\limits_{s\to 0} \dfrac{1}{s(1+GG_c)} = \dfrac{1}{\lim\limits_{s\to 0} sGG_c} & \text{for ramp input} \\ \lim\limits_{s\to 0} \dfrac{1}{s^2(1+GG_c)} = \dfrac{1}{\lim\limits_{s\to 0} s^2 GG_c} & \text{for parabolic input} \end{cases} \quad (30)$$

Eq. (30) can be rewritten in terms of the static position error constant, κ_p, the static velocity error constant, κ_v, and the static acceleration error constant, κ_a, as defined in [16] as follows:

$$\begin{aligned}\kappa_p &= \lim_{s\to 0} GG_c \\ \kappa_v &= \lim_{s\to 0} sGG_c \\ \kappa_a &= \lim_{s\to 0} s^2 GG_c\end{aligned} \tag{31}$$

As stated above, in the case of type 1 systems, where one of the poles is zero, the steady state error of the system can be stated in terms of the velocity error constant, κ_v. We have used the following system to demonstrate the lag compensator design:

$$G(s) = \frac{\alpha_1}{s(s+p_1)(s+p_2)} \tag{32}$$

The above system has no zero and three poles: 0, $-p_1$ and $-p_2$. This is a type 1 system, since it has only one pole at the origin, and hence, the steady-state error of the above system for a step input will always be zero. Let's assume the goal is to find K_{cLag}, such that the maximum steady state error due to a ramp input is e_{vss}, which corresponds to the maximum velocity error constant κ_v given by $\kappa_v=1/e_{vss}$. The following relationship can be deduced from the second relationship in Eq. (30).

$$e_{vss} = \frac{1}{\lim_{s\to 0} sGG_c} \tag{33}$$

The application of Eqs. (27), (32) and (33) yields the following:

$$e_{vss} = \frac{p_{cLag}}{z_{cLag}} \frac{p_1 p_2}{\alpha_1 K_{cKag}} \tag{34}$$

From which K_{cLag} can be deduced as

$$K_{cLag} = \frac{p_{cLag}}{z_{cLag}} \frac{p_1 p_2}{\alpha_1 e_{vss}} \tag{35}$$

Regarding the location of the pole, p_{cLag}, and zero, z_{cLag}, of the compensators, the ratio p_{cLag}/z_{cLag} must be as small as possible since the objective of the lag compensator is to minimize the steady state error. Conversely, z_{cLag}/p_{cLag} must be maximal. Therefore, there are two conditions that the zero and the pole of the lag compensator must satisfy: 1) p_{cLag} and z_{cLag} must be closed to each other, and 2) the ratio z_{cLag}/p_{cLag} must be maximal. The only way to satisfy these two conditions is to ensure that the compensator poles and zeros are located near zero.

3-2. Determination of the Lag Compensator Gain

After the controller's pole and zero are properly selected, the gain, K_{cLag}, of the lag compensator can be calculated as follows:

- **Type 0 systems:** a general high order SISO type 0 system given as

$$G_0(s) = \frac{K\Pi_{i=1}^{m}(s+z_i)}{\Pi_{i=1}^{n}(s+p_i)} \tag{36}$$

Referring to Fig. 1, the steady state error of the delay-free system for a unit step input can be found as follows:

$$e_{ss} = \frac{\Pi_{i=1}^{n} p_i}{\Pi_{i=1}^{n} p_i + KK_{cLag} \frac{z_{cLag}}{p_{cLag}} \Pi_{i=1}^{m} z_i} \tag{37}$$

Hence, the gain of the lag compensator can be deduced as

$$K_{cLag} = \frac{p_{cLag}}{z_{cLag}} \frac{\Pi_{i=1}^{n} p_i}{K\Pi_{i=1}^{m} z_i} \frac{1-e_{ss}}{e_{ss}} \tag{38}$$

- **Type 1 systems:** a general high order SISO type 1 system given as

$$G_1(s) = \frac{K\Pi_{i=1}^{m}(s+z_i)}{s\Pi_{i=1}^{n}(s+p_i)} \tag{39}$$

Using Eq. (33), the following relationship can be deduced for type 1 systems

$$\lim_{s\to 0} sGG_c = \frac{1}{e_{vss}} \Rightarrow KK_{cLag} \frac{\Pi_{i=1}^{m} z_i}{\Pi_{i=1}^{n} p_i} \frac{z_{cLag}}{p_{cLag}} = \frac{1}{e_{vss}} \tag{40}$$

And hence, the gain of the lag compensator can be deduced as follows:

$$K_{cLag} = \frac{p_{cLag}}{z_{cLag}} \frac{\Pi_{i=1}^{n} p_i}{\Pi_{i=1}^{m} z_i} \frac{1}{Ke_{vss}} \tag{41}$$

The proposed design algorithm of the lead-lag compensator of the SISO high order system can be summarized as follows:

- Performance specifications are given in the time domain (desired settling time, damping ratio, maximum overshoot, etc.)
- Calculation of the desired pole location, s_d, as shown in Eqs. (12) and (13)
- Calculation of the compensator angle of the lead compensator, θ_c, as in Eq. (20)
- Calculation of the position of the zero of the lead compensator, z_{cLead}, as in Eq. (21)
- Calculation of the location of the pole of the lead compensator, p_{cLead}, as in Eq. (24)
- Calculation of the gain of the lead compensator, K_{cLead}, as in Eq. (25)
- Calculation of the lead controller, G_{Lead}, as in Eq. (26)
- Specification of the maximum steady state error and the system type
- Location of the zero z_{cLag} and the pole p_{cLag} of the lag compensator near the origin. The distance between the zero and the pole can be used as a tuning parameter, so long as the pole and zero do not drift far from zero.
- Calculation of the gain of the lag compensator, K_{cLag}, as in Eqs. (38) and (41), depending on the system type.
- Calculation of the lag compensator, G_{Lag}, as in Eq. (27)
- Calculation of the lead-lag compensator, $G_{LeadLag}$, according to Eq. (2)

Based on the above design of the lead-lag compensator, the control gain K_P, K_I and K_d of conventional PID controller can be obtained, as described in the next subsection.

DESIGN OF THE PID CONTROLLER FROM THE LEAD-LAG COMPENSATOR

As mentioned, lead-lag compensators are general forms of con-

ventional PID controllers. Indeed, a PD controller can be derived from the lead part of the lead-lag compensator, while the lag part can be used to design a PI controller, providing a PID in the form of PI and PD controllers in cascade. In this section, a PID controller is designed utilizing the lead-lag compensator design technique. A conventional PID controller can be described as follows:

$$G_{PID}=K_P+\frac{K_I}{s}+K_D s=\frac{K_D s^2+K_P s+K_I}{s} \tag{42}$$

PID controllers can be realized by aligning a PD controller in cascade with a PI controller. Let the PD part of the PID controller be given as

$$G_{PD}=K_{PD}(s+z_{PD}) \tag{43}$$

And the PI part of the PID controller be given as

$$G_{PI}=K_{PI}\frac{s+z_{PI}}{s} \tag{44}$$

The PID controller in Eq. (42) can then be re-written as follows:

$$G_{PID}=G_{PD}G_{PI}=K_{PD}K_{PI}\frac{(s+z_{PD})(s+z_{PI})}{s} \tag{45}$$

By comparing Eqs. (42) and (45), the proportional, integral and derivative gain of the controller K_P, K_I and K_D can be found as follows:

$$\begin{aligned} K_D&=K_{PD}K_{PI}\\ K_I&=K_{PD}K_{PI}z_{PD}z_{PI}\\ K_P&=K_{PD}K_{PI}(z_{PI}+z_{PD}) \end{aligned} \tag{46}$$

After designing K_{PD}, z_{PD}, K_{PI} and z_{PI} using the lead-lag compensator technique, the gain of the PID can be determined by using Eq. (46). Referring to Fig. 5, z_{PD} can be determined using the following:

$$z_{PD}=s_{s_d}-\frac{y_{s_d}}{\tan(\pi-\theta_c)}=x_{s_d}+\frac{y_{s_d}}{\tan\theta_c} \tag{47}$$

with θ_c calculated as in Eq. (20). $x_{sd}=\mathrm{Re}(s_d)$ is the real part of the desired closed-loop pole s_d and $y_{sd}=\mathrm{Im}(s_d)$ is its imaginary part.

Following the same steps used to obtain Eq. (25), K_{PD} can be obtained as

$$K_{PD}=\frac{\Pi_{i=1}^{n}|s_d+p_i|}{|K||s_d+z_{PD}|\Pi_{i=1}^{m}|s_d+z_i|}\frac{|s+p_{DT}|}{|s-z_{DT}|} \tag{48}$$

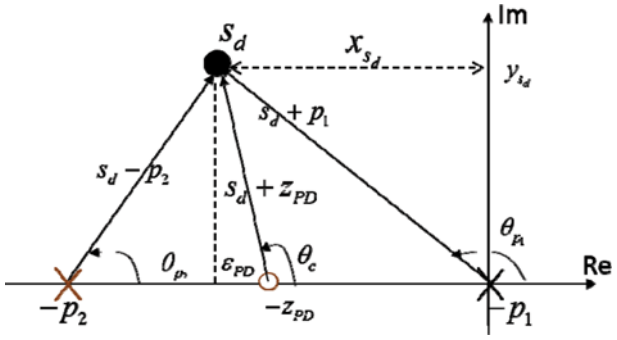

Fig. 5. Location of the pole and zero of the PD compensator.

The only remaining parameters required to calculate the PID gain parameters in Eq. (46) are the zero of the lag compensator, z_{PI}, and the gain of the lag compensator, K_{PI}. As proven in the previous section, since the compensator poles and zeros must be close to the origin for a lag compensator, z_{PI} can be placed near the origin. Furthermore, because a PI controller always brings the steady state error to zero for a step input, K_{PI} can be determined if the steady state error due to a ramp input, e_{vss}, is known. Following the same procedure which was used to obtain the K_{cLag} in Eq. (41), K_{PI} can be obtained as follows:

$$K_{PI}=\frac{\kappa_v}{Kz_{PI}}\frac{\Pi_{i=1}^{n}p_i}{\Pi_{i=1}^{m}z_i}=\frac{1}{Kz_{PI}e_{vss}}\frac{\Pi_{i=1}^{n}p_i}{\Pi_{i=1}^{m}z_i} \tag{49}$$

Now that K_{PD}, z_{PD}, K_{PI} and z_{PI} are known, the PID gain parameters K_P, K_I and K_d can be obtained from Eq. (46).

SIMULATION RESULTS

Without loss of generality, simulation results of the lead-lag compensator will be applied to the following type 0 process of third order plus dead-time with a zero:

$$G(s)=5\frac{s+1}{s^3+4.1s^2+3.4s+0.3}e^{-\theta s} \tag{50}$$

The control performance of the proposed lead-lag compensator by the proposed method will be presented, followed by that of proposed PID controller.

1. Results of the Lead-lag Compensator Design

The desired control specifications were given as follows: damping ratio, ζ=0.8; settling time, t_s=1 min; steady state error, e_{ss}=0.01. Fig. 6 shows the effect of the lead-lag compensator on the closed-loop step responses shown in Eq. (50), for a dead-time of θ=0.1 min. The proposed algorithm automatically computed the lead-lag DT-preview transfer function and yield

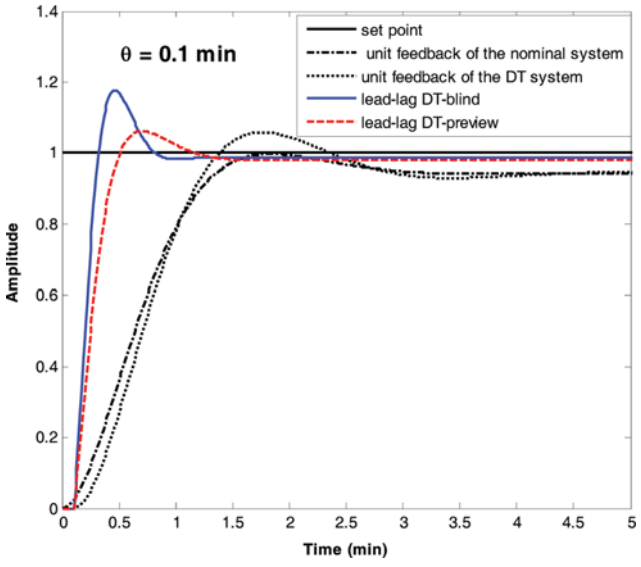

Fig. 6. Effect of the lead-lag compensator on the closed-loop step responses of the process with θ=0.1 min.

$$G_{LeadLag}=\frac{85.21s^2+346.1s+4.138}{s^2+127.8s+0.2543} \quad (51)$$

In Fig. 6, the term nominal system refers to the delay-free system, the system without dead-time. The plot named "unit feedback of the nominal system" represents the delay-free closed-loop system; the plot named "unit feedback of the DT system" represents the closed-loop of the dead-time process; the plot named "lead-lag DT-blind" represents the plot of the lead-lag controller which was designed without taking into account the dead-time term in the design stage; the plot named "lead-lag DT-preview" is the plot of the lead-lag controller which was designed by taking into account the dead-time term in the design phase. The advantage of taking the dead-time into account during the controller design phase can be clearly seen from this figure, since the system "lead-lag DT-preview" keeps the process closer to the desired specifications, as compared to the "lead-lag DT-blind" compensator. Indeed, the "lead-lag DT-preview" plot confirms the design specifications regarding the required settling time which was fixed to one minute and the steady state offset which was fixed to 0.01. The maximum overshoot, which is directly related to the damping ratio also closely matches the desired damping ratio of ζ=0.8.

As shown in Fig. 7, as the dead-time of the process increases, "lead-lag DT-blind" compensator system which is designed without taking into account the dead-time tends to quickly become oscillatory, as compared to the "lead-lag DT-preview" which does account for dead-time.

2. Results of the Automatic PID Controller Design

The desired control specifications were given as follows: damping ratio ζ=0.8; settling time t_s=1 min; since for PID the steady-state error for a step input is zero by default, it was specified the steady state error for a ramp input as e_{vss}=0.5; the zero of the PI compensator was placed to z_{PI}=0.1.

Fig. 8 shows the effect of the PID controller on the closed-loop step responses assuming dead-time-free process. The PID gain parameters that match the controller performance specifications were automatically obtained without any trial and error. As can be seen in Fig. 8, the PID controller has the fastest rise time, relatively same maximum overshoot, and cancels out the steady state error in about one minute. The PD controller for this case has a similar response with the lead-lag DT-preview controller. Referring to Figs. 8 and 9, it can be seen from the trend of the curves that, as the dead-time term increases, the PID control design will have quicker response, but tends to become quickly unstable than its corresponding lead-lag compensator. To tackle this issue, the steady state error for a ramp input, e_{vss}, can be used as a detuning coefficient for the stability of the PID controller as the dead-time increases. For higher dead-time terms, the value of e_{vss} should be increased to keep the

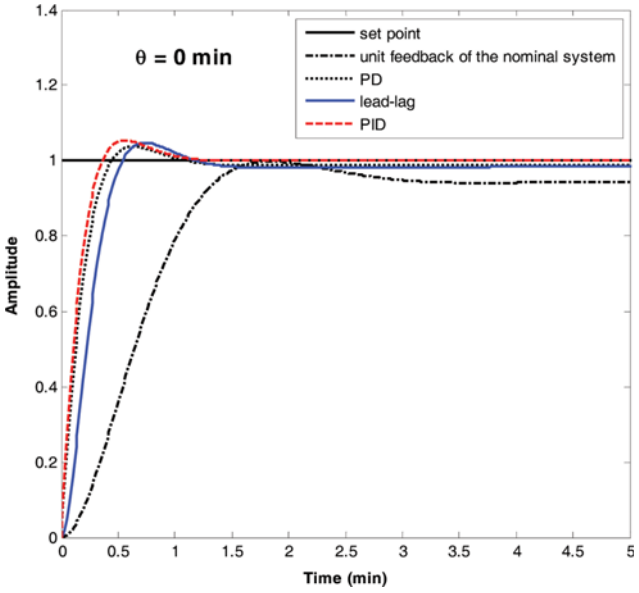

Fig. 8. Effect of the PID controller on the closed-loop step responses without dead-time.

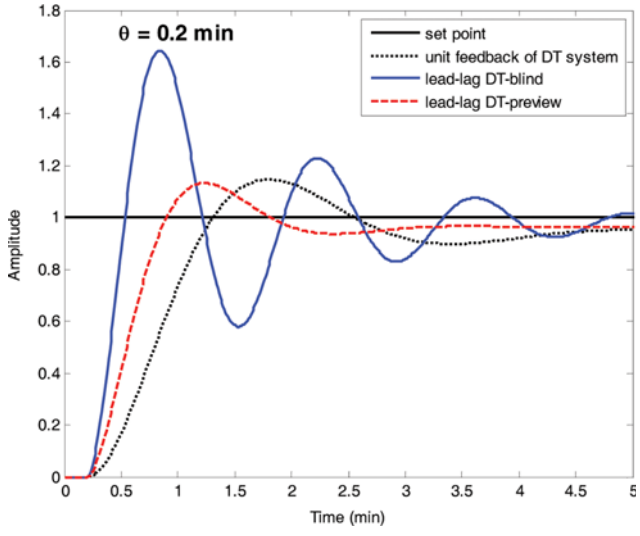

Fig. 7. Effect of the lead-lag compensator on the closed-loop step responses of the process with θ=0.2 min.

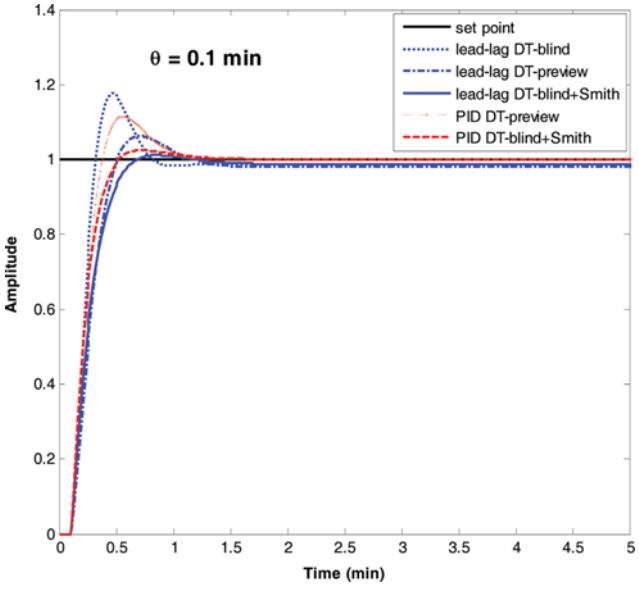

Fig. 9. Effect of the PID and Smith dead-time compensator on the closed-loop step responses with θ=0.1 min.

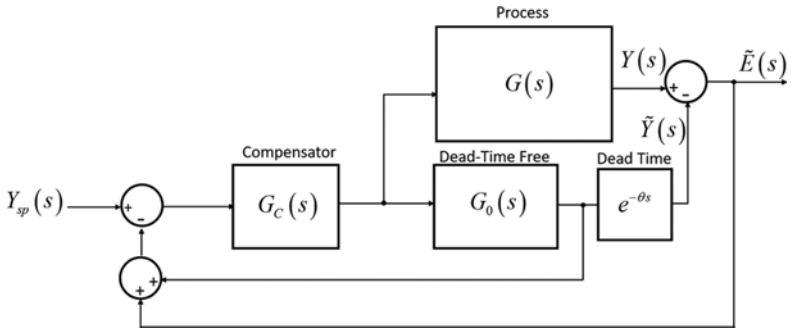

Fig. 10. Smith Predictor dead time compensator.

PID response stable, and vice versa.

It is well known that if a time delay is introduced into a well-tuned system, the gain must be reduced to maintain the overall stability of the system. To avoid redesigning the controller and improving the control performance, a well-known dead-time compensator such as the Smith predictor control can be used [33]. The Smith predictor used here is shown in Fig. 10, where Y is the actual process variable, $\tilde{Y}$ the estimated process variable, and $\tilde{E}$ the estimated process variable error. In this paper, we assumed the process model and the dead time estimation clearly match those of the real process. For more complicated cases where there is a mismatch between the model estimation and the process, interested readers can refer to [33]. The advantage of using the Smith predictor can be clearly seen in Fig. 9. As shown, the PID+Smith predictor now compensates performance degradation due to dead-time successfully and gives excellent performance over all other responses.

CONCLUSIONS

An efficient procedure and algorithm for designing PI, PD, and PID controllers for high order SISO dead-time processes was proposed. The lead-lag compensator procedure was first explained, after which a simplified procedure to automatically design PID control gains that meet control specifications in time domain was proposed. Although the design of the lead-lag and PID controller showed good result for lower dead-time, the control system can become unstable for larger dead-time. The Smith predictor can be used together with the proposed algorithm, and the results using those two combinations are far more enhanced.

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